R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

INTERVIEW SUMMARY

Applicant's representative, John Ignatowski, spoke with Examiner Whitmore via telephone on May 18, 2004 to discuss a series of questions (faxed the day before to the Examiner) regarding ambiguities for the arguments in the Office Action concerning the Uchida reference. No clarification was provided. No agreement was reached.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 6 lines 9-18 and FIG. 2 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 4, 6, 7, 9, 13-16, 21 and 22 under 35 U.S.C. §102(b) as being anticipated by Uchida et al. '304 (hereafter Uchida) has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

Uchida concerns a semiconductor integrated circuit (Title). Anticipation requires the presence in a single prior art reference disclosure of **each and every element** of the claimed invention, **arranged as in the claim** (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(Emphasis added). Uchida does not appear to disclose or suggest every element as arranged in the claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides an input pin for data and a shift register couplable to the input pin for shifting in the data. In contrast, Uchida appears to be silent regarding a bonding pad 10 (asserted similar to the claimed input pin) being couplable to the ID code register 5 (asserted similar to the claimed shift register) for shifting in data. In particular, Uchida only shows the bonding pad 10 connected to the multiplexers 41, 42 and 43 within an ID code setting portion 4 (asserted to include the claimed multiplexer). The rest of Uchida appears to be silent regarding the bonding pad 10 being couplable to the ID code register 5. Therefore, Uchida does not appear to disclose or suggest an input pin for data and a shift register couplable to the input pin for shifting in the data as presently claimed. The Examiner is respectfully requested to either (i) provide an explanation how the ID code register 5 of Uchida is couplable to the bonding pad 10 for

shifting in the data from the bonding pad 10 (e.g., how does information at the "S" input to multiplexer 41 get to the "O" output of the multiplexer 41?) or (ii) withdraw the rejection.

Claim 1 further provides that the first multiplexer has a third input for receiving a control signal that controls selection between a first input and a second input. Assuming, *arguendo*, that the bonding pad 10 of Uchida is similar to the claimed input pin (for which Applicant's representative does not necessarily agree), Uchida appears to be silent regarding another input of a first multiplexer receiving a control signal. Therefore, Uchida does not appear to disclose or suggest a first multiplexer having a third input for receiving a control signal that controls selection between a first input and a second input as presently claimed. Claims 13 and 14 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that the configuration signals are user variable. Despite the assertion on pages 3 and 7 of the Office Action, the text in column 9 lines 1-17, column 2 lines 27-28, column 2 lines 60-62 and column 10 lines 13-15 of Uchida appear to be silent regarding elements 12 and 13 being user variable.

> FIG. 7 is an illustration showing the practical detail of the bonding judgement portion, the ID code setting portion and the ID register in a still further embodiment of the present invention. In FIG. 7, the bonding judgement portion 3 comprises a decoder (DEC) 37.

> The input signal pad 12 is connected to the A-terminal of the decoder 37 and the input signal pad 13 is connected to the B-terminal of the decoder 37. The output of the decoder 37 is connected to the D-terminal of the F/F 51 and the A-terminals of the multiplexers 41 to 43, respectively.
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> In the still embodiment of the present invention, the decoder is adapted to output the ID code depending upon the levels of the signals input to the input signal pads 12 and 13 so that the ID code of the product name and so forth can be set by the levels of the signals to be input to the input signal pads 12 and 13. (Column 9 lines 2-17)
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> Among the bonding pads 115 to 118, the bonding pads 116 and 117 are used for establishing the identification code of the product name of the IC-chip per se. Namely, depending upon the connection of these bonding pads to the ten of taps, ID code can be differentiated. (Column 2, lines 23-27)
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> As set forth above, in the conventional semiconductor integrated circuit, setting of the kind code is performed at the diffusion process or writing in to the ROM. (Column 2, lines 60-62)
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> However, other four bits ID codes can be selectively output by varying the combination of the input signal levels for the input signal pads 12 and 13. (Column 10, lines 12-13)

Nowhere in the above text, or in any other section, does Uchida appear to discuss the ID code being **user variable**. In particular, the two blocks of text cited in column 2 of Uchida do not even mention the bonding pads 12 and 13. Furthermore, the assertion on page 7 of the Office Action that a ROM is user variable appears to contradict the common definition of a ROM as a read-only device having predetermined contents. Therefore, Uchida does not appear to disclose or suggest configuration signals that are user variable as presently claimed. Claim 15 provides language similar to claim 2. The Examiner is respectfully requested to either (i) provide evidence where Uchida explicitly or inherently discloses user

variability of the signals on bonding pads 12 and 13 or (ii) withdraw the rejection.

Claim 4 provides that each value of a device identification identifies a unique configuration of a circuit. Despite the assertion on pages 3 and 8 of the Office Action, the text in column 9 line 40-column 10 line 28 and column 8 line 52-column 9 line 1 of Uchida appear to be silent regarding a unique configuration of a circuit.

> Then, "1" i s output from the Q-terminal of the F/F 51, "0" is output from the Q-terminal of the F/F 52, "0" is output from the Q-terminal of the F/F 53 and "1" is output from the Q-terminal of the F/F 54. Accordingly, from the ID code output pad 8, "1" is output.
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> After the timing where "1" is output from the ID code output pad 8, the signals for the S-terminals of the multiplexers 41 to 43 of the ID code setting portion 4 from the ID code setting pad 10 are turned into low level to switch the signal to be output from the O-terminals of the multiplexers 41 to 43 to the signals input to the D-terminals.
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> Accordingly, to the D-terminal of the F/F 52 of the output ID code register 5, the output "1" from the Q-terminal of the F/F 51 is applied. To the D-terminal of the F/F 53 of the ID code register 5, the output "0" from the Q-terminal of the F/F 52 is applied. To the D-terminal of the F/F 54 of the ID code register 5, the output "0" from the Q-terminal of the F/F 53 is applied.
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> On the other hand, at rising of the next shift clock from the shift clock pad 9, The F/F 53 takes "1" from the Q-terminal of the F/F 52 provided at the D-terminal. The F/F 54 takes "0" from the Q-terminal of the F/F 53 provided at the D-terminal. Therefore, "1" is output from the Q-terminal of F/F 53 and "0" is output from the Q-terminal of the F/F 54. Therefore, "0" is output from the ID code output pad 8.
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> Furthermore, at the rising of the next shift clock, the F/F 54 takes "1" from the Q-terminal of the F/F 53 provided at the D-terminal. Then, from the Q-terminal of the F/F 54, "1" is output. Therefore, "1" is output from the ID code output pad 8.

By the operation set forth above, by setting so that the ID code is output sequentially in an order from the least significant bit (LSB) to the most significant bit (MSB), the ID code "1001" can be output from the ID code output pad 8 at a third rising of the shift clock from the shift clock pad 9.

In the foregoing embodiment of the present invention, discussion has been given for the case where "1001" is output from the decoder by inputting low level and high level respectively to the input signal pads 12 and 13. However, other four bits ID codes can be selectively output by varying the combination of the input signal levels for the input signal pads 12 and 13.

Also, by using the bonding judgement portion 3 as a level judgement portion, the foregoing another embodiment of the present invention can be applied for setting of the identification code for the derivative products, for which the grade of the wafer is selected by P/W selection after diffusion process.

Furthermore, by varying the ID code set in the ID code register with the output from the decoder depending upon cutting of the fuses 33 to 36 or setting of the levels of the signals applied to the input signal pads, it becomes possible to vary the ID code or the product name by the fuse option or the input signal levels. (Column 9 lines 40-column 10 line 28)

By the operation set forth above, by setting so that the ID code is output sequentially in an order from the least significant bit (LSB) to the most significant bit (MSB), the ID code "1001" can be output from the ID code output pad 8 at third rising of the shift clock from the shift clock pad 9.

In another embodiment of the present invention, the foregoing discussion has been given for the case of outputting "1001" from the decoder by cutting the fuses 33 and 36, another four bits ID code can be selectively output by selectively cutting the fuses 33 to 36.

On the other hand, by using the bonding judgement portion 3 as level judgement portion, the foregoing another embodiment of the present invention can be applied for setting of the identification code for the derivative products, for which the grade of the wafer is selected by P/W selection after diffusion process. (Column 8 line 52-column 9 line 1)

Nowhere in the above text, or in any other section, does Uchida appear to discuss **a unique configuration of a circuit** identified by the signals generated by a DEC block 37 (asserted similar to the claimed identification signal). Therefore, Uchida does not appear to disclose or suggest that each value of a device identification identifies a unique configuration of a circuit as presently claimed. Claim 16 provides language similar to claim 4. The Examiner is respectfully requested to either (i) explain what circuit of Uchida has a unique configuration as identified by the ID code value or (ii) withdraw the rejection.

Claim 6 provides a second logic gate configured to generate a second identification signal from said configuration signals. Despite the assertion on page 3 of the Office Action, the "input B" of element 37 of Uchida does not appear to be a logic gate. One of ordinary skill in the art would appear to understand "input B" according to its common name, that is, an input. Therefore, Uchida does not appear to disclose or suggest a second logic gate configured to generate a second identification signal from said configuration signals as presently claimed. The Examiner is respectfully requested to either (i) provide evidence that one of ordinary skill in the art would view an input as being the same as a logic gate or (ii) withdraw the rejection.

Claim 6 further provides generating the identification signal from a plurality of configuration signals. Assuming,

arguendo, that the "input B" of element 37 of Uchida is a logic gate (for which Applicant's representative does not necessarily agree), the input B does not appear to receive a plurality of configuration signals. In particular, the input B appears to receive only one signal. Therefore, the Examiner is respectfully requested to either (i) identify the multiple signals used by the input B to generate an identification signal or (ii) withdraw the rejection.

The assertion on page 3 of the Office Action that logic gates are inherent to decoders is respectfully traversed. MPEP §2112 states:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. " *Ex parte Levy* 17 USPQ2d 1461, 1464, 1464 (Bd. Pat. App. & Inter. 1990)(emphasis in original)

The text of the Microsoft *Computer Dictionary*, cited on page 8 of the Office Action, fails to mention logic gates in defining the term "decoder". Therefore, no evidence exists that logic gates are necessary to implement a decoder. Furthermore, the Examiner's reading of the decoder definition in the *Computer Dictionary* is opinion, not evidence. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 9 provides a FIFO memory and (from claim 1) a shift register. In contrast, Uchida appears to be silent regarding both

a FIFO memory and a shift register. Furthermore, the assertion on page 3 of the Office Action that the claimed FIFO is similar to the ID code register 5 of Uchida conflicts with the assertion on page 2 of the Office Action that the same ID code register 5 of Uchida is similar to the claimed shift register. The single ID code register 5 of Uchida cannot simultaneously anticipate two claim elements under *Lindemann Maschinenfabrik GmbH*. Therefore, Uchida does not appear to disclose or suggest at least one of (i) a FIFO memory and (ii) a shift register as presently claimed. The Examiner is respectfully requested to either (i) identify both a FIFO and a shift register in FIG. 7 of Uchida or (ii) or withdraw the rejection.

Claim 21 provides an output multiplexer configured to multiplex a device identification from a shift register to an output pin. In contrast, Uchida appears to be silent regarding an output multiplexer between the ID code register 5 and a bonding pad 8 (asserted similar to the claimed output pin). In particular, an output of the ID code register 5 of Uchida appears to be directly connected to the bonding pad 8. Therefore, Uchida does not appear to disclose or suggest an output multiplexer configured to multiplex a device identification from a shift register to an output pin as presently claimed. Claim 22 provides language similar to claim 21. The Examiner is respectfully requested to either (i) explain how the ID code setting portion 4 in FIG. 7 of

Uchida multiplexes an output from the ID code register 5 to the bonding pad 8 or (ii) withdraw the rejection.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3, 10, 12, 18 and 20 under 35 U.S.C. §103(a) as being unpatentable over Uchida in view of the Background section of the pending application is respectfully traversed and should be withdrawn.

The rejection of claims 5 and 17 under 35 U.S.C. §103(a) as being unpatentable over Uchida in view of Adams et al. '732 (hereinafter Adams) is respectfully traversed and should be withdrawn.

Uchida concerns a semiconductor integrated circuit (Title). Adams concerns a storage device capacity management (Title). Uchida, Adams and the Background Section of the application, alone or in combination, do not appear to teach or suggest every claimed element. Furthermore, *prima facie* obviousness has not been established for lack of evidence of motivation to combine the references and a reasonable expectation of success.

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific

combination that was made by the applicants."[1] "[T]he factual inquiry whether to combine references must be thorough and searching."[2] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[3] "It must be based on objective evidence of record."[4] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[5] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[6]

Claim 3 provides a JTAG compliant controller. In

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[1] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[2] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[3] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[4] *Id.* at 1343, 61 USPQ2d at 1434.

[5] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003, §2142.

[6] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

contrast, page 5 of the Office Action admits that Uchida does not disclose a JTAG compliant controller. The Background Section of the application is also silent regarding a JTAG compliant controller. Therefore, Uchida and the Background Section of the application, alone or in combination, do not appear to teach or suggest a JTAG compliant controller as presently claimed. The Examiner is respectfully requested to either (i) identify by specific page and line number (e.g., not the entire Background section as cited in the Office Action) where the Background section of the application discloses a JTAG compliant controller or (ii) withdraw the rejection.

Furthermore, the asserted motivation on page 6 of the Office Action to combine Uchida with the Background Section does not appear to be based on either Uchida or knowledge generally available to one of ordinary skill in the art (MPEP §2143.01). Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to either (i) identify the source of motivation to combine Uchida with the Background section of the application or (ii) withdraw the rejection.

Furthermore, the Office Action has not provided evidence of a reasonable expectation of success (MPEP §2143.01). Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success or (ii) withdraw the rejection.

Claim 5 provides that a device identification determines a storage capacity of a circuit. In contrast, page 6 of the Office Action admits that Uchida does not disclose a device identification determining a storage capacity of a circuit. Furthermore, lines 1-3 of the Abstract of Adams state that the storage medium is of "a predetermined size and corresponding capacity." Adams appears to be silent that the predetermined storage capacity is somehow variable or that the capacity is somehow governed by the device identification. Therefore, Uchida and Adams, alone or in combination, do not appear to teach or suggest a device identification that determines a storage capacity of a circuit as presently claimed. Claim 17 provides language similar to claim 5. The Examiner is respectfully requested to either (i) explain how the abstract and column 1 line 50-column 2 line 10 of Adams allegedly teaches determining a storage capacity using identification information or (ii) withdraw the rejection.

Furthermore, nowhere in the Abstract, column 1 line 50-column 2 line 10 and column 10 lines 1-44 of Adams does not appear to state that the invention of Adams would improve control over device configuration as asserted on page 7 of the Office Action. Therefore, *prima facie* obviousness has not been established for lack of clear and particular evidence of motivation. The Examiner is respectfully requested to either (i) explain how the cited text of Adams teaches improving control over device configuration or

(ii) withdrawn the rejection.

Furthermore, the Office Action is silent regarding any evidence for a reasonable expectation of modifying the IC Chip 1 of Uchida to manage RAM capacity using techniques developed by Adams for a host system managing a hard disk drive. Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to either (i) provide evidence of a reasonable expectation of success or (ii) withdraw the rejection.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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Dated: July 2, 2004

Docket No.: 0325.00374